

# PMV45EN

## N-channel TrenchMOS logic level FET

Rev. 2 — 7 November 2011

Product data sheet

## 1. Product profile

### 1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in computing, communications, consumer and industrial applications.

### 1.2 Features and benefits

- Logic-level compatible
- Trench MOSFET technology
- Very fast switching

### 1.3 Applications

- Battery management
- High-speed switching

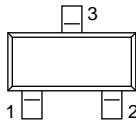
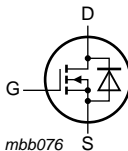
### 1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 150\text{ °C}$	-	-	30	V
$I_D$	drain current	$T_{sp} = 25\text{ °C}$ ; $V_{GS} = 10\text{ V}$ ; see <a href="#">Figure 1</a> ; see <a href="#">Figure 3</a>	-	-	5.4	A
$V_{GS}$	gate-source voltage		-20	-	20	V
<b>Static characteristics</b>						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$ ; $I_D = 2\text{ A}$ ; $T_j = 25\text{ °C}$ ; see <a href="#">Figure 9</a> ; see <a href="#">Figure 10</a>	-	35	42	mΩ

## 2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p>SOT23 (TO-236AB)</p>	 <p>mbb076</p>
2	S	source		
3	D	drain		

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## 3. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
PMV45EN	TO-236AB	plastic surface-mounted package; 3 leads	SOT23

## 4. Marking

Table 4. Marking codes

Type number	Marking code <sup>[1]</sup>
PMV45EN	%4N

[1] % = placeholder for manufacturing site code

## 5. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 150\text{ °C}$	-	30	V
$V_{DGR}$	drain-gate voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 150\text{ °C}$ ; $R_{GS} = 20\text{ k}\Omega$	-	30	V
$V_{GS}$	gate-source voltage		-20	20	V
$I_D$	drain current	$T_{sp} = 100\text{ °C}$ ; $V_{GS} = 10\text{ V}$ ; see <a href="#">Figure 1</a>	-	3.4	A
		$T_{sp} = 25\text{ °C}$ ; $V_{GS} = 10\text{ V}$ ; see <a href="#">Figure 1</a> ; see <a href="#">Figure 3</a>	-	5.4	A
$I_{DM}$	peak drain current	$T_{sp} = 25\text{ °C}$ ; pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; see <a href="#">Figure 3</a>	-	21.6	A
$P_{tot}$	total power dissipation	$T_{sp} = 25\text{ °C}$ ; see <a href="#">Figure 2</a>	-	2	W
$T_{stg}$	storage temperature		-55	150	°C
$T_j$	junction temperature		-55	150	°C
<b>Source-drain diode</b>					
$I_S$	source current	$T_{sp} = 25\text{ °C}$	-	1.7	A
$I_{SM}$	peak source current	$T_{sp} = 25\text{ °C}$ ; pulsed; $t_p \leq 10\text{ }\mu\text{s}$	-	6.9	A

## 6. Characteristics

**Table 6. Characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	30	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	27	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C$ ; see <a href="#">Figure 8</a>	1	1.5	2	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 150 \text{ }^\circ C$ ; see <a href="#">Figure 8</a>	0.6	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ C$ ; see <a href="#">Figure 8</a>	-	-	2.2	V
$I_{DSS}$	drain leakage current	$V_{DS} = 30 V; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	1	$\mu A$
		$V_{DS} = 30 V; V_{GS} = 0 V; T_j = 150 \text{ }^\circ C$	-	-	100	$\mu A$
$I_{GSS}$	gate leakage current	$V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	10	100	nA
		$V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	10	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 V; I_D = 2 \text{ A}; T_j = 25 \text{ }^\circ C$ ; see <a href="#">Figure 9</a> ; see <a href="#">Figure 10</a>	-	35	42	m $\Omega$
		$V_{GS} = 10 V; I_D = 2 \text{ A}; T_j = 150 \text{ }^\circ C$ ; see <a href="#">Figure 9</a> ; see <a href="#">Figure 10</a>	-	59.5	71.4	m $\Omega$
		$V_{GS} = 4.5 V; I_D = 1.5 \text{ A}; T_j = 25 \text{ }^\circ C$ ; see <a href="#">Figure 9</a> ; see <a href="#">Figure 10</a>	-	45	54	m $\Omega$
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 3 \text{ A}; V_{DS} = 15 V; V_{GS} = 10 V;$ $T_j = 25 \text{ }^\circ C$ ; see <a href="#">Figure 11</a>	-	9.4	-	nC
$Q_{GS}$	gate-source charge		-	1.2	-	nC
$Q_{GD}$	gate-drain charge		-	1.9	-	nC
$C_{iss}$	input capacitance	$V_{DS} = 30 V; V_{GS} = 0 V; f = 1 \text{ MHz};$ $T_j = 25 \text{ }^\circ C$	-	350	-	pF
$C_{oss}$	output capacitance		-	70	-	pF
$C_{rss}$	reverse transfer capacitance		-	50	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 15 V; R_L = 15 \Omega; V_{GS} = 10 V;$ $R_{G(ext)} = 6 \Omega; T_j = 25 \text{ }^\circ C$	-	5	-	ns
$t_r$	rise time		-	7	-	ns
$t_{d(off)}$	turn-off delay time		-	16	-	ns
$t_f$	fall time		-	5.5	-	ns
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 1.5 \text{ A}; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$ ; see <a href="#">Figure 12</a>	-	0.79	1.2	V